

The monolithic phase-locked loop

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A review of the principle of operation of the phase-locked loop, its applications, practical realisation and a close look at some of the integrated circuits available to the system designer.

Phase-locked loops have a wide range of applications in radio reception, in motor speed control, in various types of instruments, etc, whilst they are especially useful for stereo signal decoding.

The principle of operation of a phase-locked loop has been known for over 40 years,¹ but phase-locked loops using discrete components tend to be so complex that one usually avoids them if other circuits offering a similar performance are available for the application concerned.

Various types of monolithic phase-locked loops have been available since the early 1970s. A single device can replace almost the whole of a radio receiver i.f. amplifier and demodulator circuit with few external components. Stereo decoder monolithic phase-locked loops enable simple circuits to be made which have a better performance than the earlier decoders and also have the advantage that they can be adjusted very easily. Monolithic devices are being designed at the present time which offer lower noise and higher operating frequency than existing types.

Principle of operation

The principle of operation of a phase-locked loop will be illustrated using the block diagram of Figure 1. This basic circuit can itself be used to demodulate f.m. signals, but some additional circuitry is required for a.m. demodulation.

If no input signal is fed to the loop, the voltage-controlled oscillator operates at a frequency known as the 'free running' or 'centre' frequency. Under these conditions, the phase detector provides no output or error signal and there is therefore no control or error voltage fed to the voltage-controlled oscillator.

If an input signal is now fed to the phase detector, the latter will compare the phase of the input signal with that of the signal from the voltage-controlled oscillator. An error voltage is thus produced which is dependent on the phase difference between the two signals. In general, the error signal may be either positive or negative, depending on which of the two signals is leading in phase.

The error signal is passed through a low pass filter which removes any of the high frequency oscillations and is then amplified before being used to control the frequency of the local oscillator. The control voltage is of such a polarity that it

brings the output of the local oscillator closer to the input frequency. If the input frequency is close enough to the centre frequency, the local oscillator will become locked in frequency to the input signal, but, in general, there is a small phase difference between the two signals; indeed, it is this very phase difference which generates the error signal.

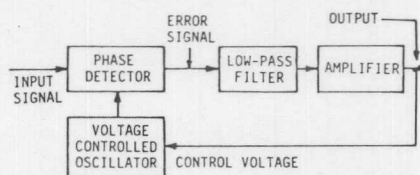


Figure 1. A basic phase-locked loop in block form.

The feedback circuit of a phase-locked loop automatically causes the local oscillator frequency to change so that the latter is always equal to the input frequency. However, this process will occur only when the input frequency is within the 'locking range' or 'holding range' of frequencies on each side of the centre frequency. The locking range is limited by the maximum control voltage which can be generated by the phase detector circuit, since this imposes a limit on the frequency range of the voltage-controlled oscillator. The locking range can be many times the bandwidth of the signals accepted by the loop. Thus, as the frequency of the input signal varies somewhat, the local oscillator frequency will follow it, but the bandwidth will always be limited so that noise is reduced.

The capture range is the range of input signal frequencies which can cause the loop to become locked from an initially unlocked state. In general, the capture range is smaller than the locking range, but can never exceed the locking range. The capture range defines how close in frequency the input signal must be to the centre frequency to produce locking, whilst the locking range is a measure of how far the input frequency can depart from the centre frequency before the loop comes out of lock.

The low-pass filter

The low-pass filter often consists of a series resistor with a capacitor down to ground at its output side, but sometimes one requires more complex filters. The low-pass filter affects the capture range, but not the locking range.

If an input signal which is steadily approaching the centre frequency is applied to an unlocked loop, the difference frequency generated by the phase detector decreases until it can pass through the low-pass filter and cause the local oscillator to be brought nearer to the input frequency. This reduces the difference frequency and the latter therefore suffers still less attenuation by the low-pass filter. Thus, the loop is quickly brought into lock. This capture effect determines the selectivity of the phase-locked loop.

When the loop has been brought into lock, the error voltage (due to the phase difference) is of zero frequency and will therefore pass through the low pass filter unattenuated. Thus, the filter does not affect the lock range (provided that the rate of change of the input frequency is not so great that the delay provided by the low-pass filter is important).

The low-pass filter reduces the sensitivity of the loop to stray noise pulses. Such a noise pulse will produce an almost instantaneous change in the error signal from the phase comparator. This change will be delayed by the low-pass filter; the latter thus provides a short time memory effect which keeps the local oscillator locked to the input frequency during a short noise pulse.

The low-pass filter essentially controls the selectivity of the loop. Although the filter operates at a fairly low frequency, its characteristics are effectively imposed on the high frequency response of the loop. Indeed, a simple low-pass filter can provide selectivity similar to that of a conventional superheterodyne receiver containing some six i.f. tuned circuits.

The characteristics of the low-pass filter are a compromise between the relatively low cut-off frequency required for locking to an input signal with a rapidly changing frequency. In addition, a filter with a low cut-off frequency will result in a reduced capture range and a longer pull-in time during the locking process. Phase-locked loops are especially useful for receiving radio signals with poor signal-to-noise ratios, since their pass band can be made near to the optimum.

FM reception

As the input signal of Figure 1 varies in frequency within the locking range, the error signal at the output varies in sympathy. Thus, the error signal is the re-

quired demodulated output when the input signal is frequency modulated. The local oscillator is usually designed so that its frequency is linearly related to the applied control voltage; the linearity must be good if an output with low distortion is required.

As such simple circuits can be employed as complete i.f. and demodulator subsystems, one may well ask why phase-locked loops are not more widely used in f.m. receivers for the home. Currently available monolithic phase-locked loops employ zener diodes in voltage level shifting circuits and these components render the noise level relatively high. Phase jitter also provides some noise contribution. The signal-to-noise ratio of the well-known Signetics series of high frequency phase-locked loops types NE560B, NE561B and NE562B is quoted as 35 dB. This is quite inadequate for high fidelity applications, especially in stereo equipment. However, these devices are suitable for use in communications receivers at frequencies of up to at least 15 MHz, where phase-locked loops are excellent

for recovering weak signals from a noisy input signal.

The distortion of the NE560B series of devices is typically 0.3%, but the maximum of 1% is perhaps a little high for high fidelity applications. However, it is the noise level which is the main problem. We shall see how it is being overcome in

phase-locked loops for high fidelity applications.

Currently available phase-locked loops cannot operate at frequencies exceeding about 50 MHz. F.m. broadcast signals, must, therefore, be converted to a lower frequency before they can operate the loop. If a phase-locked loop eventually becomes available which can operate at frequencies of up to 100 MHz, it may be possible to construct an f.m. receiver without any frequency conversion. However, it may still be more convenient to operate the loop at a lower frequency, since gain is usually required before the loop itself.

The NE563

The NE563 device is a particularly interesting one which was introduced by Signetics over a year ago; unfortunately it has been temporarily withdrawn owing to production problems. Nevertheless, the principles of operation of NE563 circuits are novel enough to be of considerable interest.

In the circuit of Figure 2, the 10.7 MHz input signal from the front-end passes through G1 to the input of a high gain amplifier/limiter in the NE563. The gain of this limiter is typically 60 dB and the bandwidth some 22 MHz. R5 provides d.c. stabilisation of the operating point. The output from the limiter at pin 5 passes through R2 to the 10.7 MHz ceramic filter marked F. The limiter output impedance is about 270 Ω and this, when added to R2, provides the required impedance of about 330 Ω . At the other side of the filter R1 in parallel with the mixer input impedance (pin 2) of 1.25 k Ω provides the required 330 Ω . The desired band-pass characteristic of the filter will be degraded without the matching resistors.

The signal passing into pin 2 is mixed with a 9.8 MHz local oscillator signal generated by a crystal controlled circuit. The 0.9 MHz difference frequency is fed by an internal connection to the loop section of the device. The centre frequency of the loop is controlled by the value of C12, whilst the loop filter connected to pins 13 and 14 controls the bandwidth and hence the noise level. The value of R8

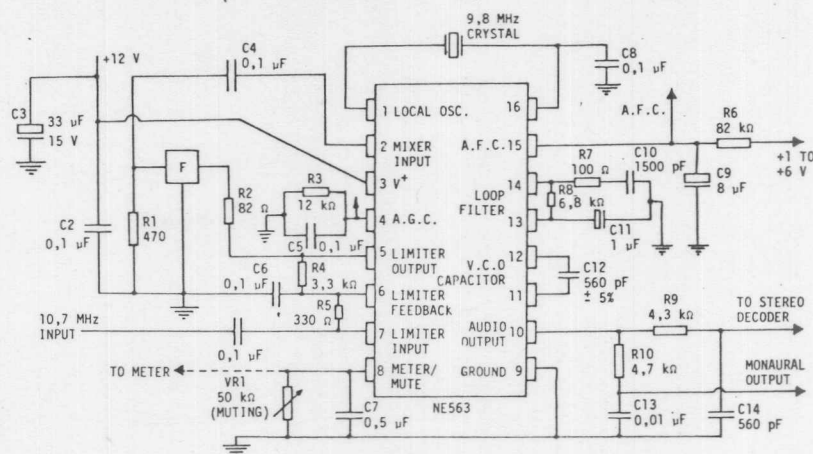
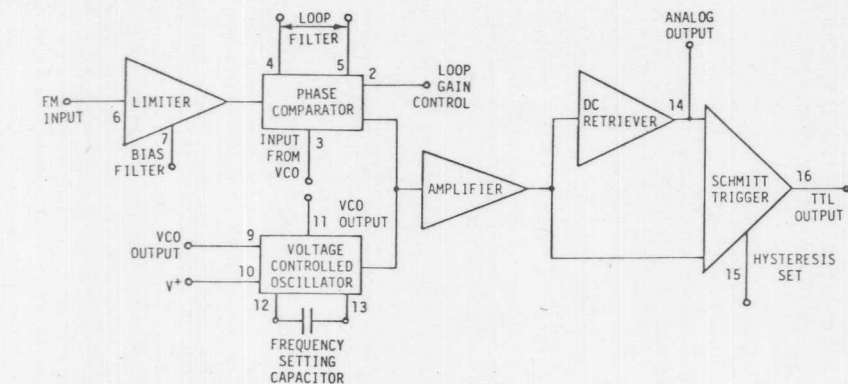
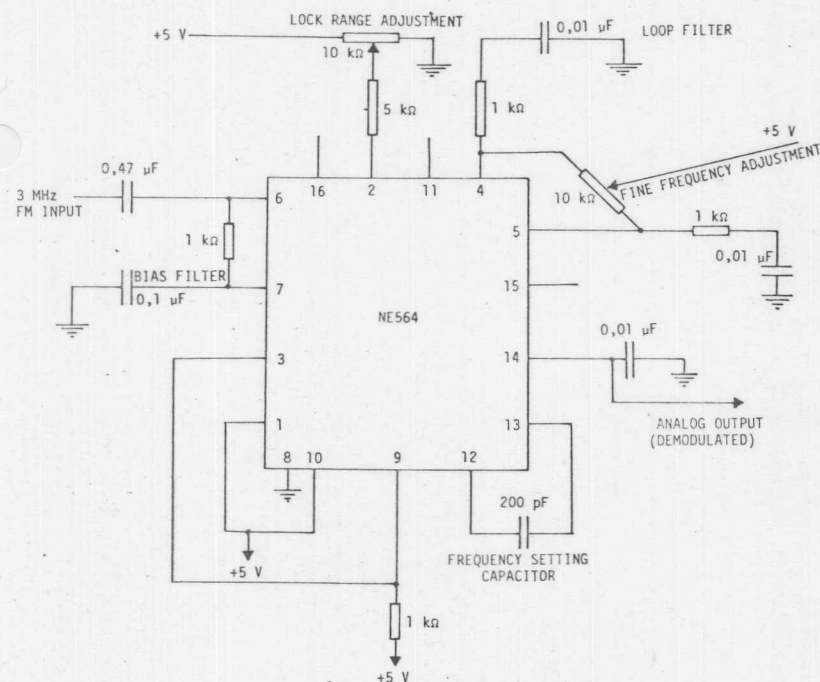


Figure 2. A typical NE563 f.m. demodulator circuit.



(a)



(b)

Figure 3. Block diagram of the NE564 device.

may be reduced if a smaller bandwidth is required for any reason. The loop filter output impedance is about 6.2 k Ω .

The output filter R9C14 attenuates radio frequencies, whilst R10C13 provides the normal 50 μ s de-emphasis for the monaural output. The effective resistance between pin 10 and ground should be not less than 2 k Ω . A series capacitor (now shown in Figure 2) will be required to pre-

the output of the whole band limiter. Reference 2 contains a full NE 563 tuner design.

The NE564

Another interesting phase-locked loop from Signetics is the NE564. The basic type of circuit for the use of the NE564 is shown in block form in Figure 3(a). The input signal passes through a limiter to improve the a.m. signal rejection after which

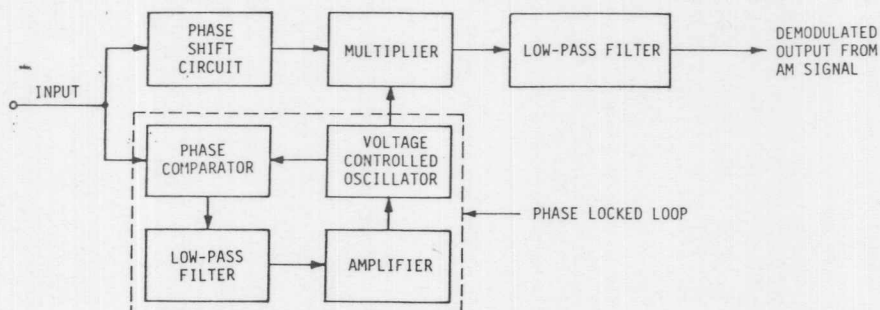


Figure 4. Block diagram of a phase-locked loop circuit for the demodulation of an a.m. signal.

vent the steady component of the voltage at pin 10 from reaching the following audio amplifier or stereo decoder.

The muting potentiometer VR1 is optional and can be used to set the interstation noise muting level. No muting takes place if pin 8 is left unconnected. If a signal strength meter is required, a high impedance voltmeter (full scale deflection about 5 V) can be connected as shown by the dotted line joined to VR1 in Figure 2. The meter reading approximates to a logarithmic function of the input signal level and is affected by the setting of VR1.

It is possible to employ certain types of ceramic resonator instead of the 9.8 MHz crystal used in Figure 2, but the writer found that the crystal gave better results, although it is more expensive.

One of the most interesting points about the Figure 2 circuit is the conversion of the signal to a lower frequency in order to increase the percentage frequency deviation. This enables a signal-to-noise ratio of about 65 dB to be obtained for input signal levels above 1 mV if a 53 kHz noise filter is employed in the output. A.m. rejection exceeds about 60 dB for input signals of over 10 mV. The total harmonic distortion is typically 0.4 % for a 75 kHz deviation and a modulating frequency of 1 kHz, the audio output being about 380 mV r.m.s. The input sensitivity is about 9 μ V (allowing for a 6 dB loss in the ceramic filter) for a 30 dB signal-to-noise ratio at 10.7 MHz.

One important point about the Figure 2 circuit is that one has a complete i.f. and demodulator circuit without any tuned circuit whatsoever. No alignment is required, although another ceramic filter may be used immediately after the front-end followed by an active amplifier to match it to the 563 limiter if optimum performance is required in a crowded f.m. band. The filter F shown in Figure 2 is required to limit the noise bandwidth at

it is passed to the phase-locked loop. The output circuit is one of the important features of the NE564, a post detection signal processor being included to provide a t.t.l. compatible output with reduced carrier frequency feedthrough. Schottky

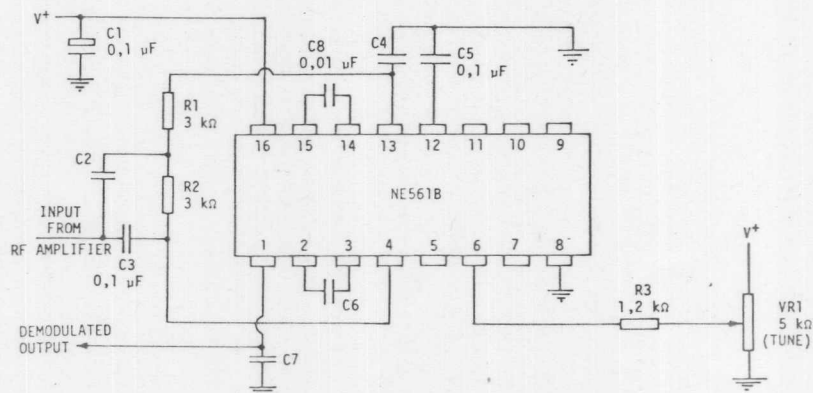


Figure 5. A practical a.m. demodulator circuit.

clamped p.n.p. transistors are employed in the output circuit to avoid the noise introduced by the zener diode level shifting circuits used in the earlier monolithic phase-locked loops. As indicated in Figure 3(a), this post detection signal processor contains a d.c. retriever and a Schmitt trigger circuit with variable hysteresis.

The NE564 will be supplied in a 16-pin dual-in-line package, like the other Signetics high frequency phase-locked loops, but will operate from a single 5 V supply in contrast to the 10 to 18 V required by the earlier monolithic devices. A typical NE564 f.m. demodulator is shown in Figure 3(b). The 200 pF capacitor connected between pins 12 and 13 sets the centre frequency of the loop to about 3 MHz. The absolute maximum permissible voltages at pins 1 and 10 are 14 V and 6 V respectively; if a 12 V supply is to be employed, the only circuit change

required is the insertion of a 1 k Ω resistor between the positive line and pin 10. The circuit shown will provide a t.t.l. compatible output from pin 16 if this pin is connected through a 4 k Ω resistor to the +5 V line. The supply current required by the circuit of Figure 3(b) is about 40 mA.

The input frequency can be as high as 50 MHz if a suitable capacitor is used in the voltage-controlled oscillator circuit and the locking range can be up to ± 50 % of the centre frequency. Frequency drift is typically 200 ppm/ $^{\circ}$ C at a 5 MHz centre frequency, whilst the drift with the power supply voltage is about 1 %/V. The output voltage is about 0.1 V peak-to-peak from pin 14 for a 1 % input frequency deviation, whilst the output linearity is typically 0.5 %. The signal-to-noise ratio for 1 % input deviation is quoted as typically 50 dB and the a.m. rejection 40 dB. The hysteresis control range of the Schmitt trigger is some 20 % to 80 %.

It is envisaged that the NE564 will be used in Citizens Band radio receivers, in signal generators, frequency shift keying (f.s.k.) transmitters and receivers, frequency synthesisers and in high speed modems. A circuit included in the provisional data sheet shows the use of the NE564 in a gated phase-locked loop demodulator circuit with t.t.l. gating pulses applied to pin

2: when this pin is 'low', the loop is out of lock. A further circuit shows its use in a modulator with a 1 kHz modulating frequency applied to pin 6 and a t.t.l. modulated output taken from pin 9; an e.c.l. modulated output is also available from pin 11.

AM demodulation

Phase-locked loops can also be used for the demodulation of a.m. signals, a block diagram of the type of circuit used for this application being shown in Figure 4. The phase-locked loop section (the parts within the dotted line) locks on to the input signal fed to it in the normal way, the voltage-controlled oscillator producing an unmodulated signal of the same frequency as the input signal. If the input signal frequency is exactly equal to the centre frequency of the loop, the two signals are 90 $^{\circ}$ out of phase.

The phase shift circuit of Figure 4

An alternative tuning method is offered by VR1 which provides a suitable bias to the fine tuning input of pin 6 so that current can either be delivered or removed

ed from this pin. For the medium-wave band, one may select C6 to make the local oscillator operate at the mean frequency used in the band (940 kHz) when the current to pin 6 is zero. The circuit should then tune the complete broadcast band with VR1; the value of R3 may be selected to give the desired tuning range.

A broadband untuned r.f. amplifier may be used before the NE561B, but care should be taken to ensure that the maximum input to the device is no greater than 0.5 V r.m.s.

Low frequency phase-locked loops

In addition to the high frequency phase-locked loops already discussed, there is a variety of low frequency loops with maximum frequencies of operation of the order of 1 MHz. One of the best-known of these devices is the 565 available from National Semiconductor and Signetics as a 14-pin dual-in-line package and also as TO-99 circular metal packages. The voltage-controlled oscillator used in this device is also available as the 566 device and has a maximum operating frequency of about 500 kHz. The minimum frequency is set by the maximum value of the local oscillator capacity which can reasonably be used; with a 10 000 μF capacitor, one can obtain about 0,001 Hz. The supply voltage range is $\pm 5\text{ V}$ to $\pm 12\text{ V}$.

Metal detector

The use of a 565 phase-locked loop in a metal detector is shown in Figure 6. This circuit was designed by J. Blecksmith of California for a Signetics contest. The 200 mm diameter search coil is connected to the Colpitts oscillator circuit of TR1 which operates at about 100 kHz. The oscillator frequency is coupled to pin 2 of the 565.

A current source (TR2 and TR3) is used to supply the current to pin 8 (about 2,5 mA) which is equal to the charging and discharging current of the local oscillator capacitor in the pin 9 circuit. A 1 % change in the frequency of oscillation will produce an output of about 0,5 V from pin 7. This output voltage is compared with the reference voltage at pin 6 by the differential amplifier of TR4 and TR5 which drives a centre reading meter. Separate controls are provided for ad-

justing the meter zero and the sensitivity.

If the search coil is brought near to a non-ferrous metal object, the frequency of oscillation will rise. However, any object containing iron will increase the inductance of the search coil and will reduce the frequency of oscillation; it will therefore cause the reading to change in the opposite direction.

Various other 565 device applications are given in references 3 and 4.

The 567

The 567 is a frequency decoding phase-locked loop which produces an output whenever a sustained frequency is present at its input which can keep the loop in the locked condition. The input frequency can be in the range of 0,01 Hz to 500 kHz. This device can be used for the detection of ultrasonic signals from an ultrasonic transducer, for the detection of low radio frequency signals or for the detection of electrical oscillations of suitable frequencies. It is encapsulated in an 8-pin dual-in-line package, although circular metal packages are also available.

The output at pin 8 of the 567 is an uncommitted collector of a small internal power transistor which can accept currents of up to 100 mA; the output can be made t.t.l. compatible.

COS/MOS p.l.l.

The CD4046 COS/MOS phase-locked loop was first introduced by RCA, but is now second-sourced by other manufacturers. Its most important feature is a very low power consumption (70 μ W typical at 10 kHz with a 5 V supply). This is over one hundred times less than that required by most bipolar phase-locked loops. The

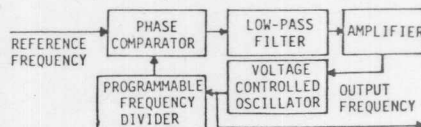


Figure 7. Frequency synthesiser.

maximum operating frequency is about 500 kHz, whilst the high input impedance of about $1\text{ T}\Omega$ is a useful feature of this device.

Apart from low frequency f.m. demodulation, the 4046 devices have important applications in frequency synthesisers.³ Frequency synthesisers are required for use in radio communications when any one of many frequencies must be generated at the touch of a button. Large numbers of quartz crystals can be used to generate these frequencies, but it is much more economical to employ a phase-locked loop containing a programmable frequency divider circuit between the voltage-controlled oscillator and the phase comparator (Figure 7). Only devices such as the 4046 and the NE562, which have facilities for the insertion of a frequency divider, can be used in this application.

In Figure 7 the local oscillator operates at a much higher frequency than the incoming reference signal. As the frequency division factor is changed, the output fre-

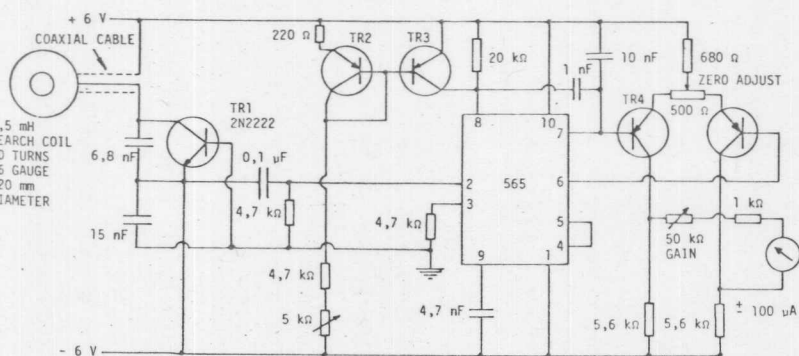


Figure 6. A metal detector using the 565 phase-locked loop device. TR2 to TR5 may be any small signal, low current p.n.p. silicon planar transistors.

Low	High	4 and 5	$1/CR + 1/CR_6$
High	Low	6	$1/CR_6$
High	High	6 and 7	$1/CR_6 = 1/CR_7$

frequency changes so that the two frequencies being fed to the phase comparator remain identical. The stability of the output frequency is determined only by the stability of the reference frequency. If the reference frequency is 1 kHz and the division factor is 121, the output will be 121 kHz.

The SL652C

The SL652C is a new monolithic phase-locked loop manufactured by Plessey Semiconductors of Swindon, England. This 16-pin dual-in-line device has been developed from the 24-pin SL650 and SL651 Plessey devices, but has most of the SL651 connections. The SL652C can be used in a wide variety of phase-locked loop circuits and for the generation of precise waveforms of frequencies up to at least 200 kHz. The maximum frequency of oscillation is typically 500 kHz, whilst the oscillator mark-to-space ratio is between 0.98 and 1.02.

The SL652C operates from a supply of ± 6 V (absolute maximum ± 7.5 V) at a typical current of only 1.5 mA. The input required by the phase comparator to maintain the loop in lock is typically 1 mV.

The basic internal circuit of the SL652C is shown in Figure 8. If no connection is made to pins 8 and 9, the current switches are in the states shown. The frequency control current, I , therefore passes only through the resistor R connected to pin 5. The frequency of oscillation in kHz is equal to $V_R/(CRV_1)$ where V_1 and V_R are the negative voltages at the points shown in the circuit, R is in kilohms and C is the value of the timing capacitor in μ F. If the timing resistor R is returned to the same negative line as pin 1, $V_R = V_1$ and the frequency is equal to $1/CR$. A frequency range of 100:1 can be accommodated with a single timing capacitor. The typical temperature coefficient is $2 \times 10^{-5}/^\circ\text{C}$, but is typically $2.5 \times 10^{-6}/^\circ\text{C}$ over the limited temperature range 0°C to 40°C at 1 kHz with a timing current of 60 μ A ($C = 10$ nF, $R = 100$ k Ω and power supplies of ± 6 V).

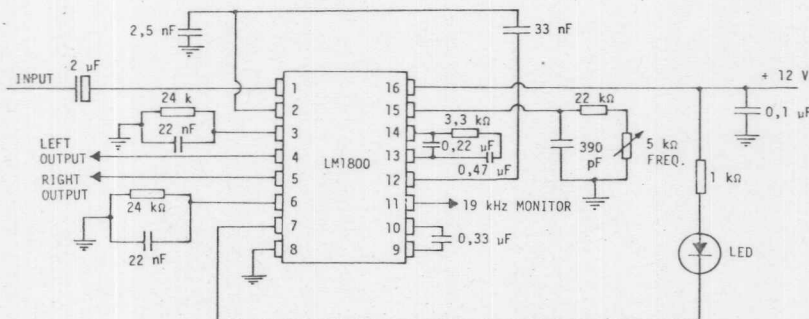


Figure 9. A typical circuit for a phase-locked stereo decoder, using the LM 1800.

However, the SL652C variable frequency oscillator can be programmed to operate at any one of four spot frequencies by means of a binary interface circuit with inputs at pins 8 and 9. These inputs accept standard t.t.l. pulses which control the switches S1 to S4 inclusive and hence the current I . When no connection is made to pin 8 or pin 9, these inputs are kept in the 'low' state and only S2 is closed; thus the current I is determined by the value of the single resistor in the pin 5 circuit. The other three frequencies can be selected by raising the potential of either pin 8 or pin 9 or both to a minimum of +2.4 V. The frequencies thus obtained are shown in the Table. The input currents to pins 8 and 9 have a maximum value of 2.5 μ A (typical 0.05 μ A).

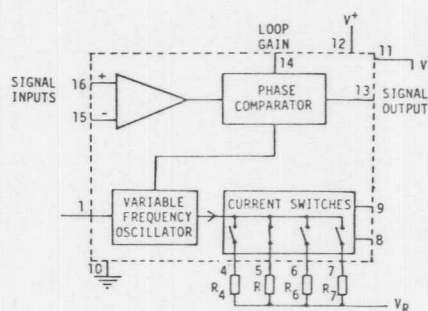


Figure 8. SL652C block diagram.

The timing current, I , from the variable frequency oscillator should be between 20 μ A and 2 mA for optimum performance. This corresponds to a value of R from 3 to 500 k Ω when ± 6 V supplies are used. The value of CR should exceed 5 μ s for accurate timing.

Stereo decoders

A monolithic phase-locked loop is now an accepted part of a modern stereo decoder circuit. The first device of this type to become available was the RCA CA3090 in 1971, but this has been replaced by an improved version, the CA3090AQ. It requires the use of a 2 mH inductor for the tuning of the loop, but exhibits better temperature stability than inductor-less

tor. Equivalent devices such as the National Semiconductor LM1310 and the Texas Instruments SN76115N are available, followed by another type in which 45 dB of hum rejection was incorporated into the circuit in addition to the emitter follower outputs. The circuit for one device of this type, the LM 1800, is shown in Figure 9.

The voltage-controlled oscillator of a stereo decoder operates at 76 kHz and is locked to the fourth harmonic of the 19 kHz pilot tone which is present on stereo broadcasts. This enables the 38 kHz sub-carrier to be regenerated and decoding to take place. Further details of the operation of the LM1800 are given in reference 6.

When the circuit of Figure 9 operates in the stereo mode, the light-emitting diode is illuminated. If the 19 kHz pilot tone is switched off during a monaural transmission, or if the signal (including the pilot tone) becomes so weak that satisfactory stereo reception is impossible, the circuit automatically switches to the monaural mode for maximum signal-to-noise ratio and the diode is extinguished. The components in the pin 3 and pin 6 circuits are the de-emphasis components.

When the circuit is first used, the 5 k Ω potentiometer should be adjusted for the correct local oscillator centre frequency. This may be carried out by feeding the output from pin 11 to a frequency counter, but one can also feed a weak stereo signal to the device and adjust the potentiometer for the mid-point of the part of its track over which locking occurs as indicated by the light-emitting diode.

Conclusion

Phase-locked loops are used for a wide variety of applications of which only a few have been briefly reviewed here. Nothing has been said of their use in television receiver 'jungle' circuits, whilst readers requiring information as to how the speed of electric motors can be locked to a stable reference frequency should consult a Motorola folder (reference 7).

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